SYSTEM AND METHOD FOR ADDING AN INSTRUCTION TO AN INSTRUCTION SET ARCHITECTURE

Abstract of the Disclosure

A processor comprising a feature indicator associated with at least one of a first sequence of one or more instructions, a first register, a second register, and an execution core is provided. The execution core is configured to execute a second instruction to cause the first register to be set to a first value using the feature indicator and to cause the second register to be set to a second value using the feature indicator. The execution core is configured to execute the first sequence of one or more instructions to cause a function to be performed in response to the first value in the first register indicating a true condition, and the execution core is configured to execute a second sequence of one or more instructions to cause the function to be performed in response to the second value in the second register indicating the true condition.